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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,792	08/29/2001	Paul A. Farrar	M4065.0382/P382-A	5268

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,792	FARRAR ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-48,51-56,58-60,62-65,67-74 and 76-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-48,51-56,58-60,62-65,67-74 and 76-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

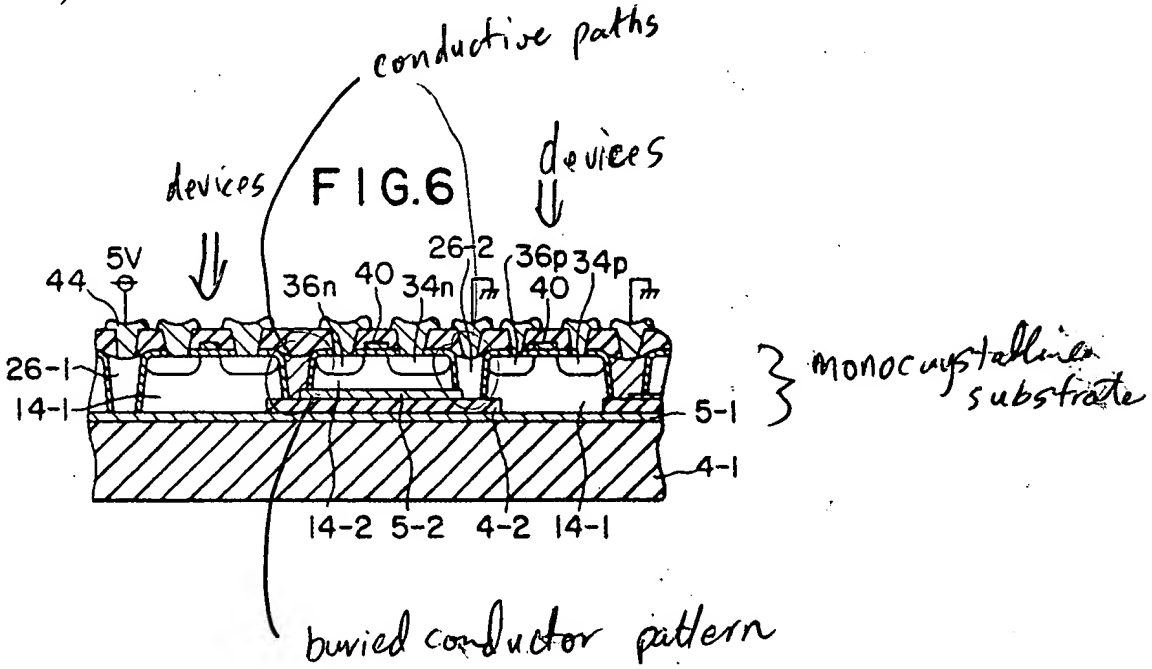
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 46, 51, 52, 54, 56, 58, and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Asakawa et al. 5,565,697. Asakawa discloses (see, for example, FIG. 6) a semiconductor device (integrated circuit substrate) comprising a tungsten film (buried conductor pattern) 5-2, monocrystalline silicon film region (monocrystalline substrate) 14-1, MOSFETs (devices), and conductive paths.

Regarding claim 54, see, for example, FIG. 6 wherein Asakawa discloses a silicon oxide film (insulator substrate) 4-1.



Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 47, 48, 72, 73, 76 thru 79, and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 as applied to claims 46, 51, 52, 54, 56, 58, and 59 above, and further in view of Kenney 5,583,368. Asakawa does not disclose a second buried conductor pattern having a pipe-shaped or plate-shaped pattern, a plurality of buried conductor patterns (claim 72), and said first buried conductor pattern being located below said second buried conductor pattern (claim 76). However, Kenney discloses (see, for example, FIG. 1g) subsurface structures (for contacts to and connectors between devices) comprising trenches of varying depths. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second buried conductor pattern having a pipe-shaped or plate-shaped pattern, and said first buried conductor pattern being located below said second buried conductor pattern in order to form multiple contacts within a semiconductor device and form greater circuit integration.

In addition, the use of a plate-shaped or pipe-shaped pattern or any other combination of patterns within the same device does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

5. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 as applied to claims 46, 51, 52, 54, 56, 58, and 59 above, and further in view of Witek et al. 5,291,438. Asakawa does not disclose said monocrystalline substrate being a germanium substrate. However, germanium is one of many conventional materials used in the fabrication of semiconductor devices. In column 3, lines 63-65, Witek discloses germanium as a substrate material. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a germanium substrate in order to support a semiconductor device in a substrate because it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

6. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 as applied to claims 46, 51, 52, 54, 56, 58, and 59 above, and further in view of Choi 6,215,158 B1. Asakawa does not disclose said monocrystalline substrate being a silicon-on-nothing substrate. However, forming a substrate on nothing is one of many conventional methods of forming a semiconductor device. In FIG. 6, Choi discloses a substrate 610 on nothing with MOSFETS formed therein. It would have been obvious to one of ordinary skill in the art at the time of invention to use a silicon-on-noting substrate in order to form a semiconductor device without forming another layer which would increase manufacturing time and cost.

7. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 as applied to claims 46, 51, 52, 54, 56, 58, and 59 above, and further in view of Sato et al. "A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration." Asakawa does not disclose a sphere-shaped configuration. However, Sato discloses (see, for example, column 2, lines 4-7) a spherical pattern as one of many patterns that are formed within a substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a sphere-shaped configuration or a spherical pattern in order to form a buried pattern that supports semiconductor devices under the surface of a substrate.

Also, the use of a spherical pattern does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

8. Claim 62 thru 64, and 67 thru 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 as applied to claims 46, 51, 52, 54, 56, 58, and 59 above, and further in view of Tsu et al. 6,294,420 B1. Asakawa does not disclose a processor system and a circuit coupled to said processor. However, Tsu discloses (see, for example, FIG. 4C and FIG. 6) a memory array comprising a processor coupled to additional circuitry. In column 8, lines 61- column 9, line 7, Tsu states that the memory array may be embedded into a larger integrated circuit device wherein the memory array is included with control circuitry on the same

integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a processor system and a circuit coupled to said processor in order to utilize the device in memory circuits.

9. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 in view of Tsu et al. '420 B1 as applied to claims 62-64, and 67-71 above, and further in view of Sato et al. "A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration." Asakawa in view of Tsu does not disclose a sphere-shaped configuration. However, Sato discloses (see, for example, column 2, lines 4-7) a spherical pattern as one of many patterns that are formed within a substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a sphere-shaped configuration or a spherical pattern in order to form a buried pattern that supports semiconductor devices under the surface of a substrate.

Also, the use of a spherical pattern does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

10. Claims 74, and 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. '697 in view of Kenney '368 as applied to claims 47, 48, 72, 73, 76-79, and 81 above, and further in view of Sato et al. "A New Substrate Engineering for the Formation of

Empty Space in Silicon Induced by Silicon Surface Migration." Asakawa in view of Kenney does not disclose a sphere-shaped configuration or a spherical pattern. However, Sato discloses (see, for example, column 2, lines 4-7) a spherical pattern as one of many patterns that are formed within a substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a sphere-shaped configuration or a spherical pattern in order to form a buried pattern that supports semiconductor devices under the surface of a substrate.

Also, the use of a spherical pattern does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA).

11. Claims 76 thru 79, and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. 5,963,838 in view of Bai et al. 5,861,340 in view of Kenney 5,583,368. Yamamoto discloses (see, for example, FIG. 47) an integrated circuit substrate comprising a substrate 21, and bottom rectangular-shaped wiring layer (buried conductor pattern) 32. The bottom rectangular-shaped wiring layer is completely surrounded by the substrate, and forms an interconnect between MOS transistor (devices) 34a. A conductive path from the bottom rectangular-shaped wiring layer extends to said MOS transistors. A portion of the conductive path extends below a top surface of said substrate.

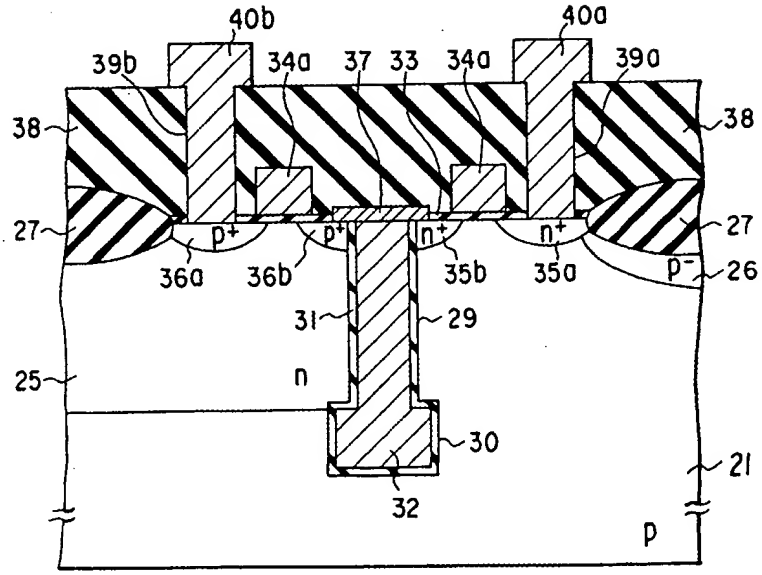


FIG. 47

Yamamoto does not disclose a monocrystalline substrate. However, Bai discloses (see, for example, column 3, lines 34-36) a monocrystalline substrate. It would have been obvious to one of ordinary skill in the art at the time of invention to have a monocrystalline substrate in order to have a substrate with less crystal defects.

Yamamoto in view of Bai does not disclose a second buried conductor pattern having a pipe-shaped or plate-shaped pattern, and said first buried conductor pattern being located below said second buried conductor pattern. However, Kenney discloses (see, for example, FIG. 1g) subsurface structures (for contacts to and connectors between devices) comprising trenches of varying depths. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second buried conductor pattern having a pipe-shaped or plate-shaped pattern, and said first buried conductor pattern being located below said second buried conductor pattern in order to form multiple contacts within a semiconductor device and form greater circuit integration.

In addition, the use of a plate-shaped or pipe-shaped pattern or any other combination of patterns within the same device does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

12. Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. '838 in view of Bai et al. '340 in view of Kenney '368 as applied to claims 76-79, and 81 above, and further in view of Sato et al. "A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration." Yamamoto in view of Bai in view of Kenney does not disclose a sphere-shaped configuration or a spherical pattern. However, Sato discloses (see, for example, column 2, lines 4-7) a spherical pattern as one of many patterns that are formed within a substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a sphere-shaped configuration or a spherical pattern in order to form a buried pattern that supports semiconductor devices under the surface of a substrate.

Also, the use of a spherical pattern does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA

Response to Arguments

13. Applicant's arguments with respect to claims 46-48, 51-56, 58-60, 62-65, 67-74, and 76-81 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
October 16, 2005